A Fully Differential Synchronous Demodulator for AC Signals

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***Abstract*— A novel fully differential (FD) demodulator is presented. Using different design strategies, the circuit can be used for processing amplitude-modulated (AM) signals obtained from impedance measurements or coming from modulating sensors with differential outputs where a high common-mode rejection ration (CMRR) and low noise are demanded. The circuit multiplies the AM input signal by a square wave with the same frequency and phase of the carrier of the input signal. This kind of wave is simpler to generate than a sine wave (homodyne detection) and narrow unit-amplitude pulses (synchronous sampling). The proposed circuit is not a perfect floating system, but yields a high CMRR if matched op-amps are used and does not depend on matched resistors. The system has been tested with off-the-shelf amplifiers; at 100 kHz, the CMRR is about 65 dB when fast and wide-bandwidth amplifiers are used. The spectral density of noise voltage obtained is lower than 55 nV/$\sqrt{}$Hz at 1 kHz; for a bandwidth of 15 Hz, this results in a noise voltage (rms) of 213 nV. Provided the circuit is implemented with low value resistors, the main contribution of noise comes from the noise voltage of the op-amps used to implement the demodulator.**

***Index Terms*— Coherent demodulation, common-mode rejection ratio (CMRR), fully differential (FD), low-noise, synchronous demodulator.**

I. Introduction

RESISTIVE and variable reactance sensors supplied by an ac voltage or impedance measurements yield amplitude-modulated (AM) signals with very low amplitude, where the information is contained in the amplitude or the phase of the modulating component. For example, linear variable differential transformers (LVDT) are widely used sensors in industrial, even in medical applications for measuring physical quantities such as displacement, force, or pressure. These sensors must be unconditionally supplied by an alternating voltage (or current), where the physical quantity modulates the amplitude of the voltage (or current) supplied. One of the main advantages of LVDTs is that they provide a differential output that must be connected to a differential-input system in order to take out the information of interest (i.e., the modulating component). Another example is related to bioimpedance measurements, where the basal impedance of some tissues is AM by the dynamic activity of some physiological functions, for example, from the arterial blood circulation [1]. Variations of 500 mΩ have been reported, which demanded a fully differential (FD) demodulation in order to reduce the contribution of common-mode (CM) errors caused by the electrode impedance imbalances and the finite CM rejection ratio (CMRR) of the measurement system [2].

Phase-sensitive (synchronous or coherent) demodulation is the technique commonly employed to recover both the amplitude and phase from an AM signal, where the input signal is multiplied by a reference wave with the same frequency and phase of the carrier. A common method is the homodyne detection, where the reference signal is a sine wave, but it is necessary to use analog multipliers to recover the modulating component. Although these analog multipliers include differential inputs, the majority of the proposed methods work with single-ended (SE) signals, for example, as is presented in [3] and [4]. Alternatives approaches are the use of switched detectors that multiply the AM signal by a square wave or by a train of very narrow unit-amplitude pulses [5]. Also, there are available digital demodulators based on digital signal processors [6], field-programmable gate array [7], [8], and application specific integrated circuits, which have been implemented using FD synchronous demodulators [9]. The performance of digital demodulators depends on the quality of analog-to-digital conversion (ADC) and the sampling frequency. The amplitude errors are reduced by using reference sine waves computed with high accuracy [10], which requires complex programing language. For increasing the CMRR and the sensitivity of the measurement system, most of the digital demodulators are driven by differential or FD analog input amplifiers [9].

Analog synchronous demodulation has demonstrated to be a technique, not only cheap and robust but also effective [4]. They have demonstrated a good performance when the AM signals come from high-impedance sensors (capacitive) [4] or dry electrodes in bioimpedance measurements [2], also in high-resolution measurements in order to detect the cardiac activity [11], [12]. Different analog demodulator circuits have been proposed. There are those that rely on a switched-gain amplifier with SE input and output that uses an analog switch to synchronously change the gain from $+1$ to -1 [13], but a differential-to-single-ended conversion is needed in a previous stage. To address this, a differential synchronous

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demodulator with an improved CMRR has been proposed [14]. The circuit relies on a single op-amp, which makes it a good option for low-power applications, but it needs to include four analog switches to control different time phases required for demodulating the input signal. The CMRR is about 15 dB at 100 kHz and depends on a resistor connected in series with the negative input of the op-amp, necessary to determine the differential gain of the circuit. For improving this low CMRR, an additional resistor (with a specific value) in series with the positive input of the op-amp must be added.

The FD circuits are preferred because they have a larger dynamic range than their SE counterparts. With the current analog-to-digital converters with differential inputs, it is not necessary to use the differential to SE blocks. Moreover, the FD circuits are the best choice for low-power consumption and high CMRR applications [15]. In the case of demodulator circuits, FD synchronous demodulators have been proposed in order to reduce the contribution of nondesirable CM errors that could disturb the demodulated signal. For example, Koukourlis *et al.* [16] demodulated two sine waves using two parallel stages based on noncoupled switched capacitors and an instrumentation amplifier (IA). As the IA operates at low-frequencies, it is presumable that the demodulator has a high CMRR; however, the preceding noncoupled stage requires matched capacitors so as to not degrade the overall CMRR [17]. In addition, the offset of the two parallel demodulators require a very exact balance; otherwise, errors would arise [16]. Pallas-Areny and Casas [5] proposed a floating-capacitor technique to build a FD synchronous demodulator. The technique is based on synchronous sampling, where the AM signal is multiplied by a train of very narrow unit-amplitude pulses. The circuit acts as FD sampler, which takes advantage of the improved CMRR for coupled stages. However, the train of pulses has many spectral "windows" that are open to noise, and the noise equivalent bandwidth of the synchronous sampler increases for large values of the carrier frequency. Hence, the need for a band-bass filter before demodulating the AM signals. This circuit has been further analyzed by Gasulla *et al.* [18] and demonstrated that the CMRR can be higher than 60 dB at 100 kHz; however, this value depends on the duty cycle of the reference wave and can be degraded if resistors (matched or not matched) are connected in series with both of the inputs of the circuit. Casanella *et al.* [19] proposed a synchronous demodulator that uses a single op-amp and a DPDT analog switch. The system is intended to be applied for autonomous sensor and can be configured as a differential or a FD circuit; however, the CMRR obtained is lower than 49 dB at 1.5 kHz at unity gain; if CM voltages are presented, this could produce in-phase and quadrature errors [5]. An analog synchronous chopping demodulator has been proposed for high-frequency (1 MHz) inductive sensors [20]. The system is based on a FD synchronous demodulator, two chopping schemes, and a FD IA working at unity gain. As the switches work at high frequency, the demodulated signal has a residual offset because of the spike of the switching; to reduce this offset, the bandwidth of the amplifier must be 2–3 times the chopping frequency.

Monolithic analog multipliers also are suitable for synchronous demodulation. The AD633, AD835, and AD698, all from Analog Devices, have been used as analog synchronous demodulators. For example, the AD633 was used for differential capacitive estimation by an analog front end that operates at full-range scale [3]; the AD835 demonstrated reliability for capacitive rotary encoders [4]; the AD698 is a good choice for fiber-optic interferometric sensors based on an LVDT [21]. Although these monolithic circuits are compacts and require minimal external components, they are not suitable for FD applications. In addition, most of them must be driven by a sinusoidal wave as a reference signal.

For FD applications, the ADA2200 from Analog Devices seems to be a good choice. This is a monolithic synchronous demodulator that includes a buffered input, a low-pass decimation filter, a programmable infinite impulse response filter, and a mixer. This circuit has been recently used to implement a portable and simple lock-in amplifier for photoacoustic measurements [22]. The versatility of this circuit is indisputable; it can be used as a tunable filter and also it can perform phase detection using a sinusoidal or a square wave as a reference signal. It has low-power consumption and has proven to be a good choice for applications that require high precision [23].

In this paper, a FD synchronous demodulator is proposed. Using some design strategies, this circuit is suitable to process the AM signal that is obtained, for example, from impedance measurements, bioimpedance measurements, and from modulating sensors with differential outputs where high CMRR and low noise are demanded. Although the proposed demodulator is not a perfect floating circuit (because it allows a connection to ground), it provides a high CMRR. The power consumption and the noise of the circuit depend on the operational amplifiers and the value of the resistors used. For example, low-noise amplifiers and low-value resistors imply low-noise contribution, but this could raise the power-consumption of the circuit; therefore, there is a tradeoff between these parameters. The circuit is obtained by mirroring a switched-gain amplifier following the method proposed in [15], where a voltage source equal to the CM input voltage is used as the ground path for the bias currents of the amplifiers. This results in an ideally infinite CMRR. In this kind of demodulator, the reference signal is a square wave which is easier to generate than unit-amplitude pulses. Moreover, a square wave is simpler to keep its amplitude constant than a sine wave (homodyne detector), but has more "windows" opened to noise that can be reduced by placing a FD bandpass filter before demodulating.

We have focus on the synchronous demodulation performed by synchronous rectification. We present the theoretical analysis to explain the principle of operation of the proposed circuit. Later, we carry out several characterizations that allow us to obtain different metrics of the proposed circuit to finally make a comparison with others proposed FD demodulators, including the monolithic solution ADA2200.

II. Synchronous Demodulation

In order to recover the information embedded in AM signals, it is necessary a method that could result in a frequency

translation that yields a baseband component. This procedure could consist in multiply the AM signal by another (reference) signal that includes the carrier frequency [13]. The circuit presented in this paper multiplies an AM input signal by a square wave, $r(t)$, that is in-phase with the carrier signal, $c(t)$, whose amplitude is modulated by a low-frequency signal, $x(t)$, which is the information of interest. Assuming a double-sideband transmitted carrier (DSBTC) AM signal, $m(t)$, which is very common in impedance and bioimpedance measurements, we have

$$m(t) = [1 + x(t)]c(t) \tag{1}$$

$$m(t) = V_c \cos 2\pi f_c t + \frac{V_x V_c}{2} \times \{\cos[2\pi(f_c - f_x)t - \emptyset_x] + \cos[2\pi(f_c + f_x)t + \emptyset_x]\} \tag{2}$$

where V_c and f_c are the peak amplitude and the frequency of the carrier, respectively; V_x, f_x, and $\emptyset_x$ are the peak amplitude, the frequency, and the phase of the modulating signal, respectively, being $f_c \gg f_x$.

The Fourier series for a square waveform with amplitude $+V_r$ and $-V_r$ is

$$r(t) = \frac{4V_r}{\pi} \sum_{0}^{\infty} (-1)^n \frac{\cos 2\pi(2n+1) f_r t}{2n+1} \tag{3}$$

which has a spectrum that consist of odd harmonics of the fundamental frequency, f_r, with decreasing amplitudes. Although these harmonics produce intermodulation components at the output of the demodulator that will be rejected by an output low-pass filter, for our calculations, we consider only the contribution of the fundamental frequency, f_r, [$n = 0$ in (3)], which results in

$$r(t) = \frac{4V_r}{\pi} \cos 2\pi f_r t. \tag{4}$$

From the multiplication of the DSBTC AM signal and $r(t)$, we obtain

$$d(t) = m(t)r(t) = [1 + x(t)]c(t)r(t) \tag{5}$$

where $d(t)$ is the demodulating signal, resulting

$$d(t) = [1 + x(t)]V_c \cos 2\pi f_c t \frac{4V_r}{\pi} \cos 2\pi f_r t. \tag{6}$$

If $f_c = f_r$

$$d(t) = [1 + x(t)]\frac{2V_c V_r}{\pi}[1 + \cos 2\pi(2f_c)t]. \tag{7}$$

An output low-pass filter rejects the high-frequency component $(2f_c)$ in $d(t)$, bringing about

$$\text{lpf}\{d(t)\} = \frac{2V_c V_r}{\pi}[1 + x(t)]. \tag{8}$$

For a double-sideband supressed carrier AM signal, which arise from bridge-type sensors and LVDTs, the result will be

$$\text{lpf}\{d(t)\} = \frac{2V_c V_r}{\pi} x(t). \tag{9}$$

Equations (8) and (9) demonstrate that $x(t)$ have been recovered scaled by a constant factor.

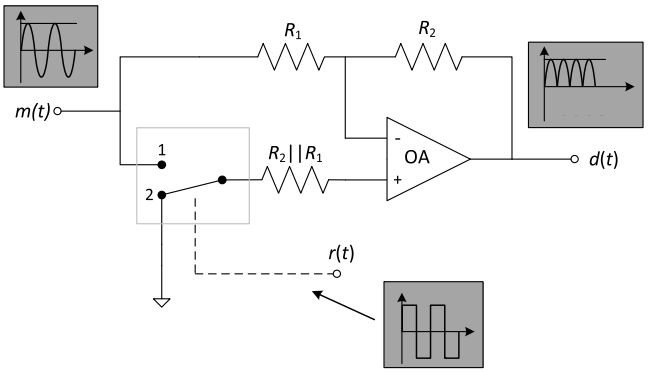

Fig. 1. SE switched-gain amplifier used as a synchronous rectifier.

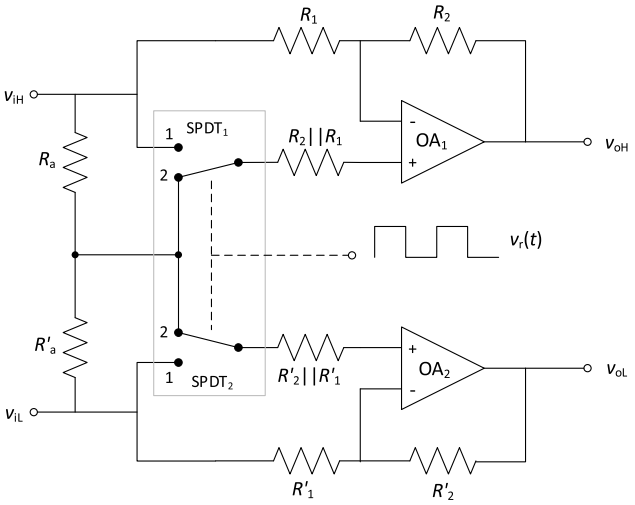

Fig. 2. Proposed FD synchronous demodulator for ac signals.

Multiplying by a square waveform in order to perform a demodulation of an AM signal reduces the procedure to a gain switching [13], which can be implemented with the circuit shown in Fig. 1. It is a SE switched-gain amplifier used as a synchronous rectifier. With this circuit, the AM signal $m(t)$ is multiplied by the square waveform $r(t)$, with amplitude $+V_r$ and $-V_r$ and frequency f_r. If $R_1 = R_2$, then $v_o = +v_i$, and $v_o = -v_i$ when the SPDT switch [controlled by $r(t)$] is in positions 1 and 2, respectively, producing a full-wave rectified signal at the output of the amplifier. This circuit is also called phase-sensitive detector because it can detect polarity changes [24].

III. Proposed Circuit

Fig. 2 shows the proposed FD demodulator, which merges from mirroring the SE circuit represented in Fig. 1. The ground path for the bias currents of the amplifiers is through a voltage source equal to a CM voltage (v_{iC}), obtained from the averaged net R_a–R'_a. This net is connected to a high-impedance node; no matter the value selected for R_a–R'_a, it does not degrade the CM input impedance, but it does degrade the differential-mode input impedance, which is not a problem if the input of the circuit is buffered by analog amplifiers. Both SPDT_1 and SPDT_2 switches are controlled simultaneously by $V_{\text{r}}(t)$,

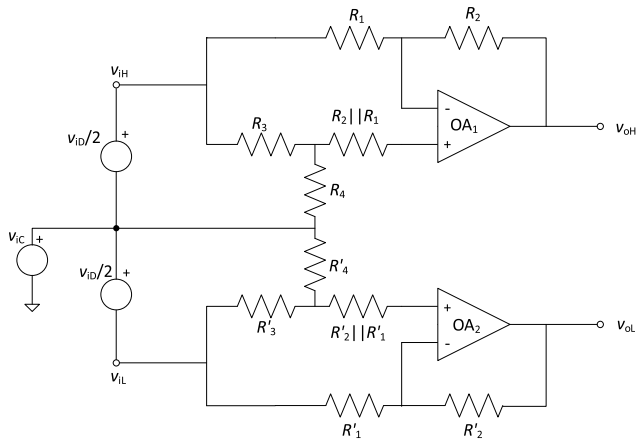

Fig. 3. Equivalent circuit of the FD synchronous demodulator used to estimate the CMRR.

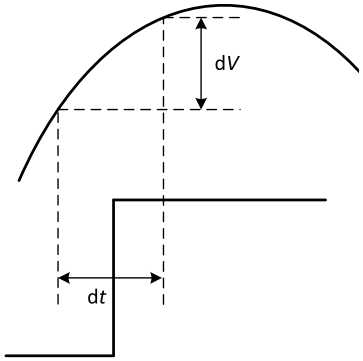

Fig. 4. Voltage error versus aperture jitter [26].

that can be obtained from a voltage comparator driven by the input carrier. Here, if $R_1 = R_2 = R'_1 = R'_2$, $v_{oD} = v_{iD}$ when $SPDT_1$ and $SPDT_2$ are in position 1, while $v_{oD} = -v_{iD}$ when $SPDT_1$ and $SPDT_2$ are in position 2; $v_{iD} = v_{iH}–v_{iL}$ and $v_{oD} = v_{oH}–v_{oL}$. If a v_{iC} is applied at the input, the CM-to-CM gain (G_{CC}) results in unity, so as all the nodes adopt the same potential, no current due to v_{iC} flows through the circuits. Although the system of Fig. 2 allows connection to ground (through v_{iC}), this is an advantage over noncoupled topologies [15].

IV. Theoretical Analysis

In order to evaluate the performance of the proposed circuit, a theoretical analysis is performed to estimate the main features of the circuit, namely, the CMRR, quadrature rejection, and spectral density of noise voltage.

A. CMRR

Fig. 3 shows the equivalent circuit used to estimate the CMRR of the FD synchronous demodulator. R_3, $R_3^{'}$, R_4, and $R_4^{'}$ are the resistances of both switches $SPDT_1$ and $SPDT_2$. The value of these resistances changes as the switches are in ON or OFF state. For example, when $SPDT_1$ and $SPDT_2$ are in position 1, $R_3 = R_3^{'} = R_{ON}$ and $R_4 = R_4^{'} = R_{OFF}$; $R_{OFF} \gg R_{ON}$. v_{iC} is the voltage obtained from the average net (R_a-$R_a^{'}$) at the input.

In FD systems, there are four transfer functions that relate the differential-mode and CM output voltages (v_{oD} and v_{oC}) with the differential-mode and CM input voltages (v_{iD} and v_{iC}) [25], where the CMRR can be estimated as

$$\mathrm{CMRR}(f) = \frac{G_{DD}(f)}{G_{DC}(f)} \tag{10}$$

where $G_{DD}(f) = v_{oD}/v_{iD}$ and $G_{DC}(f) = v_{oD}/v_{iC}$.

To estimate the CMRR of the circuit shown in Fig. 3, nonideal operational amplifiers with finite CM (A_c) and differential gains (A_d) have been considered. In the proposed circuit, the limitation of the CMRR comes from G_{DC}, since $G_{DD} \approx \pm 1$ as $SPDT_1$ and $SPDT_2$ changes from position 1 to 2. Solving the circuit of Fig. 3 for G_{DC}, we obtain (see the Appendix)

$$G_{DC}(f) = \frac{A_{d1}(f) + 3A_{c1}(f)/2}{1 + A_{d1}(f)/2 - A_{c1}(f)/4} - \frac{A_{d2}(f) + 3A_{c2}(f)/2}{1 + A_{d2}(f)/2 - A_{c2}(f)/4}. \tag{11}$$

By substituting (11) in (10), we obtain

$$\mathrm{CMRR}(f) = \frac{1}{\frac{A_{d1}(f)+3A_{c1}(f)/2}{1+A_{d1}(f)/2-A_{c1}(f)/4} - \frac{A_{d2}(f)+3A_{c2}(f)/2}{1+A_{d2}(f)/2-A_{c2}(f)/4}}. \tag{12}$$

At frequencies lower than the corner frequency of the CMRR, $A_d(f) \gg A_c(f)$, therefore,

$$\mathrm{CMRR}(f) \approx \frac{A_{d1}(f)A_{d2}(f)/4}{A_{d1}(f) + A_{c1}(f)A_{d2}(f) - A_{d1}(f)A_{c2}(f) - A_{d2}(f)}. \tag{13}$$

Rearranging, the resulting CMRR is

$$\frac{1}{\mathrm{CMRR}(f)} = 4\left(\frac{1}{A_{d2}(f)} - \frac{1}{A_{d1}(f)} + \frac{1}{\mathrm{CMRR}_1(f)} - \frac{1}{\mathrm{CMRR}_2(f)}\right) \tag{14}$$

where $\mathrm{CMRR}_1(f) = A_{d1}(f)/A_{c1}(f)$ and $\mathrm{CMRR}_2(f) = A_{d2}(f)/A_{c2}(f)$ are the CMRR of the operational amplifiers 1 and 2, respectively. This expression is very similar to that presented in [17] for coupled input buffers in a three op-amp IA, where the CMRR only depends on the matching of the open-loop differential gains and the CMRR of both op-amps. The CMRR does not depend on matched resistors.

B. Quadrature Rejection

Quadrature rejection means that the measurement of the real part of the impedance is not affected by the imaginary part. A source for this error is the phase difference between the injected signal and the reference square wave. This difference can be due to the frequency limitation of the op-amps (slew rate, harmonic distortion, and bandwidth) and to the

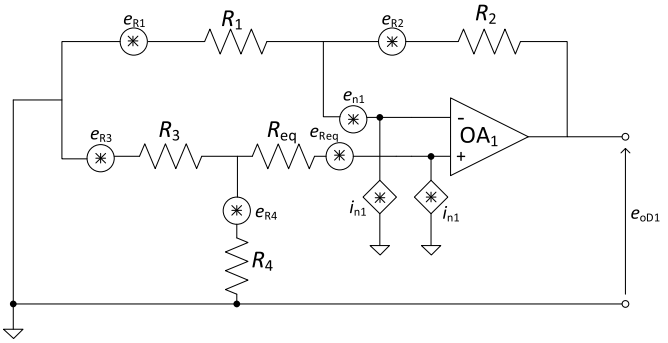

Fig. 5. Semicircuit used to estimate the PSD of noise at the output of the FD synchronous demodulator.

switches used [14]. Fig. 4 illustrates how the jitter error of the switches (dt) results in a voltage error (dV) which contributes to the uncertainty in the actual phase of the sampled signal. Therefore, we adopted the analysis presented in [26] in order to estimate how this error affects the quadrature rejection of the proposed circuit. Considering a sinusoidal input signal with and peak amplitude A and frequency f, $v(t) = A\sin(2\pi ft)$, the derivative is

$$\frac{dv(t)}{dt} = A2\pi f\cos(2\pi ft). \tag{15}$$

At $t = 0$, when the cosine equals 1 and d$v(t)$/dt is maximum, we obtain

$$\frac{dv(0)}{dt} = A2\pi f. \tag{16}$$

In order to provide a more clarity, let us define dv as ε, and dt as t_a

$$\varepsilon = A2\pi ft_a. \tag{17}$$

The quadrature rejection is degraded as the frequency increases and when using switches with high aperture jitter, resulting in nonlinearity errors [14].

C. Noise

When an AM signal is multiplied by a square wave, the noise contributed by using this kind of waveform is negligible [14]. Therefore, the main noise contribution of the proposed circuit comes from the noise sources of each op-amp and the thermal noise of the resistors. As the FD demodulator is symmetrical, the power spectral density (PSD) of noise at the output can be estimated using the semicircuit shown in Fig. 5 [27].

Considering all the sources as noncorrelated, the contribution of each noise source must be square added to estimate the differential PSD at the output. Considering $e_{oD1}(f) = e_{oD2}(f)$ [where $e_{oD1}(f)$ and $e_{oD2}(f)$ are the respective output voltage density of the upper half and the lower half of the circuit], $e^2_{oD}(f) = 2\ e^2_{oD1}(f\ )$ [27]. From the circuit of Fig. 5, if $R_1 = R_2 = R$, e_{oD} is defined by

$$e_{oD}(f) \approx 2\sqrt{\left[2e^2_{n1}(f)+2\ e^2_{teq}(f) + i^2_{n1}(f)R^2 + 2e^2_{tR}(f)\right]}(\mathrm{V}/\sqrt{\mathrm{Hz}}) \tag{18}$$

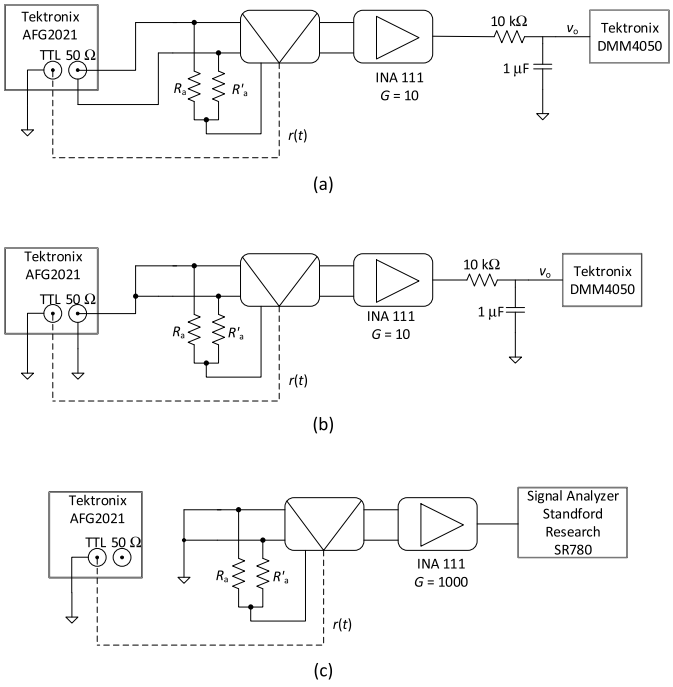

Fig. 6. Experimental setups used for characterizing the FD synchronous demodulator in order to estimate (a) G_{DD}, linearity, and quadrature rejection, (b) $G_{DC,}$ and (c) spectral density of the noise voltage. The second block on each block diagram corresponds to the circuit under test.

where $i_{n1}(f)$ and $e_{n1}(f)$ are the noise current and noise voltage densities of the op-amp 1, respectively. $e_{teq}(f\ )$ is the noise voltage density of R_{eq} ($\approx R/2$) and $e_{tR}(f)$ is the noise voltage density of R. When using resistors with low values, the contribution from i_n could be disregarded, so the noise of the proposed circuit can be lowered by using op-amps with low e_n.

D. Transient Response

When analog switches are used, a finite settling time results when switching ac signals [13]. Transients are caused due to the charge transfer between the control input and the output of the switch. That is, when the switch is ON, a charge is transferred to the output channel; when the switch is turned off, the charge must be removed. When an analog switch is connected to the input of an operational amplifier, the transient response at the output of the amplifier also depends on the bandwidth and the slew rate of the amplifier. Slow speed op-amps have a longer settling time, which generates errors at higher frequencies [19], [28]. The transient response of the amplifiers brings about systematic errors, than can be calibrated, and nonlinearity errors, which have more effects in quadrature than in-phase measurements [29]. In this paper, we have selected SPDTs with low charge transfer (10 pC) and amplifiers with different bandwidths and slew rates, so we can assess experimentally how these parameters determine the nonlinearity errors at the upper switching frequency (100 kHz).

V. Materials and Methods

Fig. 6 shows different setups used to characterize the FD synchronous demodulator. The system was battery-supplied

TABLE I
PRINCIPAL CHARACTERISTICS CONSIDERED FOR THE THREE OP-AMPS USED TO TEST THE FD SYNCHRONOUS DEMODULATOR

	TL081 (Texas Instruments)	OP27 (Analog Devices)	LT1468 (Linear Technology)	Unit
BW (min)	3	5	55	**MHz**
A_d (min)	50	600	500	**V/mV**
CMRR (min)	80	100	96	**dB**
Distortion (typ) at 100 kHz	0.2	0.03	0.001	**%**
Slew rate (min)	13	1.7	15	**V/μs**
e_n (typ) at 1 kHz	18	3.0	5.0	**nV/√Hz**
i_n (typ) at 1 kHz	0.01	0.6	0.6	**pA/√Hz**
Supply current (typ) (no load)	1.4	~2.5	6.5 (max)	**mA**

and shielded to minimize the contribution from electromagnetic interferences.

Three pairs of off-the-shelf op-amps with different characteristics were used, namely, bandwidth, slew rate, CMRR, open-loop gain, harmonic distortion, noise, and supply current (Table I). The TL081 from Texas Instruments is a general-propose amplifier; the OP27 from Analog Devices is a precision amplifier with a large open-loop voltage gain and low-noise voltage; the LT1468 from Linear Technology is a high-speed operational amplifier with low-noise voltage, wide bandwidth, and large open-loop voltage gain. $SPDT_1$ and $SPDT_2$ are two independent switches in a monolithic CMOS device (ADG436) from Analog Devices that provide a high switching speed and low ON resistances ($R_{ON} = 20\ \Omega$). The R_{ON} matching between the two switches is lower than 1 Ω. The resistors used in the demodulator were $R_1 = R_1' = R_2 = R_2' = 10\ \text{k}\Omega$ and $R_a = R_a' = 100\ \text{k}\Omega$.

An arbitrary function generator AFG2021 from Tektronix was used to supply differential [Fig. 6(a)] and common-mode [Fig. 6(b)] voltages to the input of the FD demodulator. The square wave was obtained from the TTL output of the same generator to guarantee a synchrony between the input signal and the reference wave. Also, it was possible to adjust the phase between these two signals. The output stage in Fig. 6(a) and (b) was implemented by an IA INA111 (Texas Instruments) with a gain of 10, followed by a first-order low-pass filter with a cutoff frequency of 15 Hz. This bandwidth was selected thinking of applications related to detect cardiac signals using synchronous demodulation, like those obtained in [2], [11], and [12], where a high-resolution measurement system was needed to detect low-amplitude signals buried in noise. All the measurements were obtained by a 6 ½ digits multimeter DMM4050 from Tektronix, which was configured to measure dc voltages at 1 power line cycle. None of the instruments used were connected to any PC or laptop to reduce additional electromagnetic interference; the data were storage in a USB memory for further analysis.

In the systems shown in Fig. 6(a) and (b), the overall CMRR was limited by the stage with the smaller CMRR. In order to obtain the CMRR of the circuit proposed, G_{DD} and G_{DC} were estimated as follows. For G_{DD}, it was applied a differential-mode sinusoidal wave with a peak amplitude of 100 mV from 1 to 100 kHz between both inputs of the demodulator. Then, v_o was measured for each frequency. For G_{DC}, it was applied a CM sinusoidal wave with a peak amplitude of 1 V to both inputs of the demodulator using the same frequency interval to measure the contribution at v_o. When a sinusoidal wave (differential-mode or CM) was at the input of the synchronous demodulator, a full-wave rectified signal was obtained at the output of the demodulator; once this signal was low-pass filtered, a dc voltage was obtained. Therefore, before measuring G_{DD} and G_{DC}, the offset at v_o was measured for each frequency in order to calibrate the system. For measuring the offset at the output, both inputs of the demodulator were connected to ground while the reference signal controlled $SPDT_1$ and $SPDT_2$. This procedure was repeated for each pair of op-amps under test.

The phase shift between the input signal and the reference wave was adjusted to 0° and 45° to estimate the quadrature rejection. At each phase shift, the peak amplitude of the input signal was varied from 50 to 500 mV at frequencies from 1 to 100 kHz. Then, the nonlinearity error was estimated as the maximal deviation from a straight line adjusted according to the least-squares criterion. Finally, this value was related with the full-scale range (FSR) that can be obtained at the output of the circuit.

To measure the noise contribution, we used the configuration shown in Fig. 6(c). Both inputs of the FD synchronous demodulator were connected to ground, whereas the reference signal controlled both SPDT switches. A signal analyzer SR780 from Standford Research System was used to estimate the spectral density of noise voltage at the output of the demodulator. In this procedure, we removed the low-pass filter in order to not reduce the bandwidth of the circuit under test. The gain of the IA was adjusted to 1000 to minimize the input-referred noise of this amplifier. The data were storage in a USB memory for further analysis.

In order to measure the current consumption of the circuit, the dc current at the output of the voltage regulator (used to regulate the supply voltage of the circuit) was measured by a 6 ½ digits multimeter DMM4050 from Tektronix. The IA and the low-pass filter were removed from the circuit, and no load was connected to the output of the demodulator for measuring the consumption of the active components and that due to the passive components. As the power requirement of the ADG436 is about 50 μA, the measured dc current is attributed to the op-amps (Table I) and the resistors used to implement the demodulator.

VI. RESULTS

Fig. 7 shows the comparison of the CMRR of the FD synchronous demodulator for the three pairs of op-amps tested at different frequencies. At 10 kHz, the CMRR obtained for the three op-amps is higher than 73 dB; at 100 kHz, the smallest CMRR obtained was 47 dB with the precision amplifier, OP27. At the same frequency, the highest CMRR obtained was for the TL081 and for the LT1468 (~65 dB). This value is higher

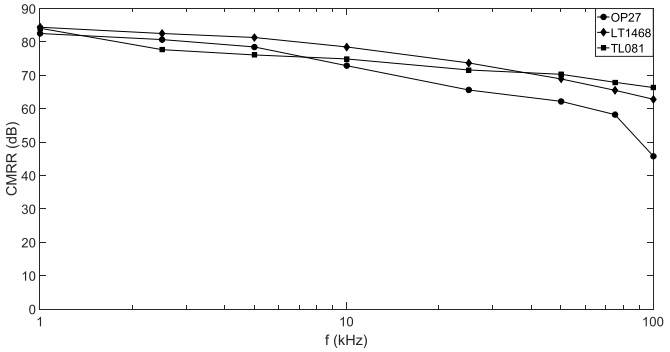

Fig. 7. CMRR of the FD synchronous demodulator measured at different frequencies for the three op-amps tested.

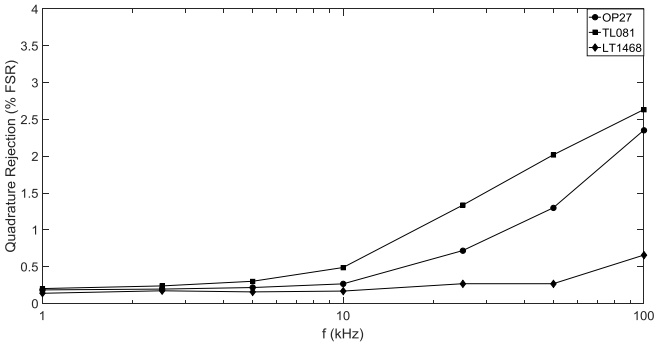

Fig. 9. Quadrature rejection expressed as a percentage of the FSR at different frequencies for the three op-amps.

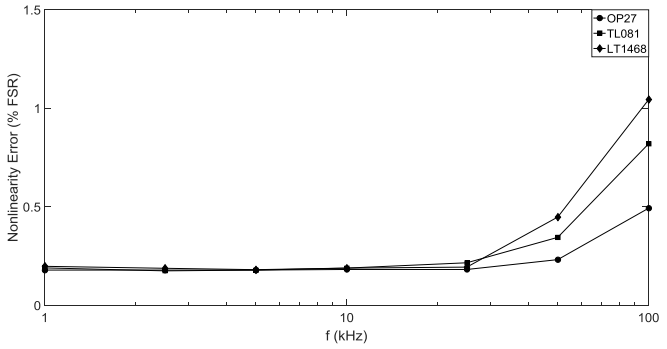

Fig. 8. Nonlinearity error expressed as a percentage of the FSR at different frequencies for the three op-amps.

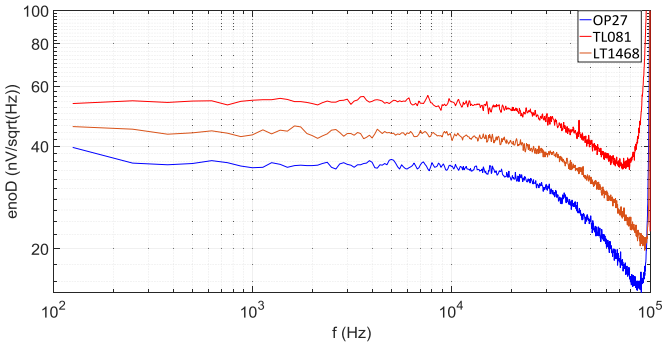

Fig. 10. Spectral density of the noise voltage of the proposed circuit when it was implemented with the three op-amps presented in Table I. Switching frequency = 100 kHz.

than that presented in [19] and is very similar to that obtained in [18]. In the former circuit, the CMRR is limited by the characteristics of the analog switch; in the latter, it is necessary to maintain the duty cycle of the reference wave at 10% for a maximal CMRR. The results shown in Fig. 7 can be attributed to the mismatch between the off-the-shelf op-amps under test, because it is very difficult to meet the condition presented in (14), since A_{d} usually start to decrease at frequencies well below the CMRR corner frequency. Specifically for the OP27, its CMRR starts to decrease at 2 kHz, well above of the corner frequency of the open-loop gain (10 Hz), so the low CMRR obtained at 100 kHz could be attributed to a high imbalance between the two off-the-shelf amplifiers at this frequency; however, the low CMRR obtained with the OP27 at 100 kHz can be increased with an input FD amplifier with high gain.

Fig. 8 shows the nonlinearity error of the FD synchronous demodulator for the three op-amps. The error was estimated as the maximal deviation from a straight line and the values are expressed as a percentage of FSR. The error increases at higher frequencies, and the largest value obtained is about 1% FSR at 100 kHz.

The proposed demodulator demonstrated to have a high quadrature rejection. Fig. 9 shows that a finite quadrature rejection will imply a nonlinear response. Nonlinearity errors are larger in quadrature than in-phase measurements and also increase as the frequency of the input signal increases, as predicted in (17). Since the slew rate of the op-amp used

TABLE II

SPECTRAL DENSITY OF THE NOISE VOLTAGE OF THE PROPOSED CIRCUIT SWITCHING AT 100 kHz. COMPARISON BETWEEN THE RESULTS OBTAINED WITH (18) AND THE EXPERIMENTAL RESULTS

	e_{noD} (nV/$\sqrt{\mathrm{Hz}}$) @ 1 kHz	
	(18)	Fig. 10
TL081 (Texas Instruments)	63	55
OP27 (Analog Devices)	38	35
LT1468 (Linear Technology)	39	43

can result in nonlinearity, it might be expected a large error from the precision (OP27) op-amp, but as shown in Fig. 9, it is probably that the large harmonic distortion and the errors due to the lower bandwidth of the TL081 predominate at 100 kHz. The lower error in quadrature was obtained for the amplifier with the largest slew rate and bandwidth. From Figs. 8 and 9, it can be said that the proposed circuit has the same limitations of linearity and quadrature rejection that are presented in other demodulator circuits that use analog switches.

Fig. 10 depicts the spectral density of noise voltage at the output of the proposed demodulator for a switching frequency of 100 kHz. The major noise contribution at 1 kHz was 55 nV/$\sqrt{\mathrm{Hz}}$, about 213 nV of rms noise voltage in a bandwidth of 15 Hz. This value was obtained when the circuit was

TABLE III
COMPARISON OF SOME METRICS OF DIFFERENT FD DEMODULATOR CIRCUITS

Parameter	Proposed circuit	Koukourlis et al. [16]	Gasulla et al. [18]	Casanella et al. [19]	Rahal et al. [20]	ADA2200
CMRR (dB)	65@100kHz	67@30 kHz	65@100kHz	49	58dB@1MHz[c]	75@1kHz
e_n (nV/√Hz)	55@1 kHz[a]	n/a	1 mV[b]	n/a	21	3500@1kHz[d]
I_{CC} (mA)	7[e]	n/a	n/a	n/a	< 1	.48
Linearity (%FSR)	1@100kHz	< 1	0.09@1kHz	0.8@15kHz	n/a	n/a
Quadrature rejection (%FSR)	2.6@100kHz	n/a	n/a	n/a	n/a	n/a

[a]Switching at 100 kHz, [b]Switching at 1 kHz, [c]Only the IA, [d]Switching at 500 kHz, [e]Using high power-consumption op-amps.

implemented with the TL081 op-amp, which has the higher noise voltage of the three op-amps tested. As the circuit was implemented with resistors with low values, the major noise contribution was due to noise voltage; the lower the noise voltage of the op-amps, the lower is the noise at the output of the demodulator. Table II shows a comparison between the results obtained from (18) and those obtained experimentally.

Finally, in Table III, we compare several metrics of our demodulator with some analog FD synchronous demodulators and the monolithic solution ADA2200. The demodulator proposed in this paper shows a CMRR at 100 kHz that is higher than that offered by the ADA2200 at 1 kHz and comparable with that obtained by Gasulla *et al.* [18], as long as the duty cycle of their reference signal is adjusted at 10%. The noise voltage density at 1 kHz was lower than 55 nV/$\sqrt{}$Hz when the switching frequency was 100 kHz. This noise contribution is much lower than the ADA2200, which has 3500 nV/$\sqrt{}$Hz at 1 kHz when it is switching at 500 kHz. Our circuit had an elevated current consumption (7 mA), but it can be reduced provided that low or ultralow power op-amps and high-value resistors are used, although this would increase the noise contribution of the circuit.

VII. CONCLUSION

A novel FD synchronous demodulator has been proposed. The circuit is based on mirroring an SE switched-gain amplifier that acts as a synchronous rectifier. The reference signal is a square wave, which is easier to keep its amplitude constant than a sinusoidal wave used in homodyne detectors and it is easier to generate than very narrow unit-amplitude pulses used in demodulators based on synchronous sampling. Although the FD demodulator is not a perfect floating system, the main advantage of the proposed circuit is the high CMRR at high frequencies. The CMRR depends on the use of well-matched operational amplifiers, and do no not depend on matched resistors, nor the characteristics of the SPDT switches. When precision operational amplifiers were used, the CMRR obtained was 46 dB at 100 kHz, which can be increased with a previous FD stage with certain gain. At the same frequency, the highest CMRR (∼65 dB) was obtained when fast and wide-bandwidth operational amplifiers were used. The proposed circuit has the same limitations of linearity and quadrature rejection reported in other demodulator circuits that use analog switches; the nonlinearity errors are higher in quadrature measurement than that obtained in-phase measurement, and increase as the frequency of the input signal and the aperture error of the SPDTs increase. The nonlinearity error was about 1% FSR at 100 kHz when the phase between the carrier and the reference wave was 0°. The system has a good quadrature rejection, where the nonlinearity error depends on the dynamic characteristics of the amplifiers used, such as slew rate, gain–bandwidth product, and harmonic distortion. It is not necessary to adjust the duty cycle of the square wave for increasing the signal-to-noise ratio, as it needed in the FD demodulator based on floating-capacitor technique. The noise voltage density is lower than 55 nV/$\sqrt{}$Hz. Since the resulting noise from multiplying a sinusoidal input signal by a square wave is lower than 1 dB, the main noise contributions come from the thermal noise of the resistors and the noise voltage and the current noise of the operational amplifiers used. Nevertheless, the contribution from the current noise and the thermal noise can be minimized by using resistors with low value, but this could bring about a power consumption increasing. Our proposal demonstrated to have a good performance at high switching frequency with regard to the CMRR and the noise contribution, when it was compared with others proposed FD synchronous demodulators.

APPENDIX

A. Effects of the Mismatch of the Operational Amplifiers on the CMRR

The connection to ground of the proposed circuit is made by a voltage source that equals to the CM input voltage, so the G_{DC} is 0 regardless on components mismatch [15]; however, it is limited by the mismatch of the op-amps used. Considering the nonideal model of the operational amplifiers, where A_d and A_c have finites values and the amplifiers are not matched, v_{oH} and v_{oL} result in (A.1) and (A.2) shown at the top of the next page.

Since $G_{DD} = \pm 1$ depending on the state of both switches, we solve (A.1) and (A.2), in order to estimate G_{DC} because this is the gain that limit the value of the CMRR of the FD demodulator. Assuming that $R_1 = R_1' = R_2 = R_2'$, $R_3 = R_3'$,

$$v_{\mathrm{oH}}(f) = \frac{v_{\mathrm{iH}}\left[\left(A_{\mathrm{d1}}(f)+\frac{A_{\mathrm{c1}}(f)}{2}\right)\left(\frac{R_4}{R_3+R_4}+\frac{R_3}{R_3+R_4}\right)-\left(A_{\mathrm{d1}}(f)-\frac{A_{\mathrm{c1}}(f)}{2}\right)\frac{R_2}{R_1+R_2}\right]+v_{\mathrm{iL}}\left[\left(A_{\mathrm{d1}}(f)+\frac{A_{\mathrm{c1}}(f)}{2}\right)\frac{R_3}{R_3+R_4}\right]}{\left[1+\left(A_{\mathrm{d1}}(f)-\frac{A_{\mathrm{c1}}(f)}{2}\right)\frac{R_1}{R_1+R_2}\right]} \quad \text{(A.1)}$$

$$v_{\mathrm{oL}}(f) = \frac{v_{\mathrm{iL}}\left[\left(A_{\mathrm{d2}}(f)+\frac{A_{\mathrm{c2}}(f)}{2}\right)\left(\frac{R_4^{'}}{R_3^{'}+R_4^{'}}+\frac{R_3^{'}}{R_3^{'}+R_4^{'}}\right)-\left(A_{\mathrm{d2}}(f)-\frac{A_{\mathrm{c2}}(f)}{2}\right)\frac{R_2^{'}}{R_1^{'}+R_2^{'}}\right]+v_{\mathrm{iH}}\left[\left(A_{\mathrm{d2}}(f)+\frac{A_{\mathrm{c2}}(f)}{2}\right)\frac{R_3^{'}}{R_3^{'}+R_4^{'}}\right]}{\left[1+\left(A_{\mathrm{d2}}(f)-\frac{A_{\mathrm{c2}}(f)}{2}\right)\frac{R_1^{'}}{R_1^{'}+R_2^{'}}\right]} \quad \text{(A.2)}$$

$$G_{\mathrm{DC}}(f) = \frac{A_{\mathrm{d1}}(f)-A_{\mathrm{d1}}(f)A_{\mathrm{c2}}(f)+A_{\mathrm{d2}}(f)A_{\mathrm{c1}}(f)+\frac{3A_{\mathrm{c1}}(f)}{2}-A_{\mathrm{d2}}(f)-\frac{3A_{\mathrm{c2}}(f)}{2}}{1+\frac{A_{\mathrm{d2}}(f)}{2}-\frac{A_{\mathrm{c2}}(f)}{4}+\frac{A_{\mathrm{d1}}(f)}{2}+\frac{A_{\mathrm{d1}}(f)A_{\mathrm{d2}}(f)}{4}-\frac{A_{\mathrm{d1}}(f)A_{\mathrm{c2}}(f)}{8}-\frac{A_{\mathrm{c1}}(f)}{4}-\frac{A_{\mathrm{d2}}(f)A_{\mathrm{c1}}(f)}{8}+\frac{A_{\mathrm{c1}}(f)A_{\mathrm{c2}}(f)}{16}} \quad \text{(A.5)}$$

$$G_{\mathrm{DC}}(f) \approx \frac{A_{\mathrm{d1}}(f)-A_{\mathrm{d1}}(f)A_{\mathrm{c2}}(f)+A_{\mathrm{d2}}(f)A_{\mathrm{c1}}(f)+\frac{3A_{\mathrm{c1}}(f)}{2}-A_{\mathrm{d2}}(f)-\frac{3A_{\mathrm{c2}}(f)}{2}}{\frac{A_{\mathrm{d1}}(f)A_{\mathrm{d2}}(f)}{4}} \quad \text{(A.6)}$$

and $R_4 = R_4'$, we obtain that

$$G_{\mathrm{DC}}(f) = \frac{1}{2}\frac{\left(A_{\mathrm{d1}}(f)+\frac{A_{\mathrm{c1}}(f)}{2}\right)-\left(\frac{A_{\mathrm{d1}}(f)}{2}-\frac{A_{\mathrm{c1}}(f)}{4}\right)}{1+\left(\frac{A_{\mathrm{d1}}(f)}{2}-\frac{A_{\mathrm{c1}}(f)}{4}\right)} - \frac{\left(A_{\mathrm{d2}}(f)+\frac{A_{\mathrm{c2}}(f)}{2}\right)+\left(\frac{A_{\mathrm{d2}}(f)}{2}-\frac{A_{\mathrm{c2}}(f)}{4}\right)}{1+\left(\frac{A_{\mathrm{d2}}(f)}{2}-\frac{A_{\mathrm{c2}}(f)}{4}\right)} \quad \text{(A.3)}$$

$$G_{\mathrm{DC}}(f) = \frac{A_{\mathrm{d1}}(f)+\frac{3A_{\mathrm{c1}}(f)}{2}}{1+\left(\frac{A_{\mathrm{d1}}(f)}{2}-\frac{A_{\mathrm{c1}}(f)}{4}\right)} - \frac{A_{\mathrm{d2}}(f)+\frac{3A_{\mathrm{c2}}(f)}{2}}{1+\left(\frac{A_{\mathrm{d2}}(f)}{2}-\frac{A_{\mathrm{c2}}(f)}{4}\right)}. \quad \text{(A.4)}$$

Solving (A.4) leads to (A.5), as shown at the top of this page.

At frequencies lower than the corner frequency of the CMRR, $A_{\mathrm{d}} \gg A_{\mathrm{c}}$, resulting (A.6), as shown at the top of this page.

Assuming $G_{\mathrm{DD}} = 1$ and substituting G_{DC} in (10), the CMRR is defined by

$$\mathrm{CMRR}(f) \approx \frac{1}{4}\left(\frac{1}{\frac{1}{A_{\mathrm{d2}}(f)}-\frac{1}{A_{\mathrm{d1}}(f)}+\frac{A_{\mathrm{c1}}(f)}{A_{\mathrm{d1}}(f)}-\frac{A_{\mathrm{c2}}(f)}{A_{\mathrm{d2}}(f)}}\right). \quad \text{(A.7)}$$

Rearranging, we obtain

$$\frac{1}{\mathrm{CMRR}(f)} \approx 4\left(\frac{1}{A_{\mathrm{d2}}(f)}-\frac{1}{A_{\mathrm{d1}}(f)}+\frac{1}{\mathrm{CMRR}_1(f)}-\frac{1}{\mathrm{CMRR}_2(f)}\right) \quad \text{(A.8)}$$

which is a very similar result obtained in [17] for FD amplifiers with coupled stages, where the CMRR is limited by the imbalances in the CMRRs and open-loop gains of the op-amps used.

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